

**AMENDMENTS TO THE CLAIMS:**

1. (Currently amended) A method for reducing capacitance between interconnect lines, the method comprising:
  - providing a substrate having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon;
  - forming a metal layer over said substrate;
  - forming a pad oxide layer over said metal layer;
  - ~~patterning~~ patterning and etching said pad oxide layer and metal layer to constitute said interconnect lines over said substrate;
  - forming an inter-metal dielectric layer over said substrate having said interconnect lines formed thereon, wherein at least an air gap is formed in a spacing between the adjacent interconnect lines; and
  - planarizing said inter-metal dielectric layer.
2. (Original) The method according to claim 1, wherein said metal layer is formed from materials selected from the group consisting of Al, Cu, Ta, W, Si, Au, Pb and Sn.
3. (Currently amended) The method according to claim 1, wherein the thickness of said pad oxide layer is between about 2000 ~~angstrom~~ angstrom and about 5000-  
angstrom ~~angstrom~~ angstrom.
4. (Original) The method according to claim 1, wherein said pad oxide layer

comprises SiO<sub>2</sub>, deposited by atmospheric pressure CVD method.

5. (Original) The method according to claim 1, wherein said pad oxide layer comprises SiO<sub>2</sub>, deposited by plasma enhanced CVD method.

6. (Currently amended) The method according to claim 1, wherein said inter-metal dielectric layer comprises a SiO<sub>2</sub> layer, deposited by plasma enhanced CVD method, utilizing TEOS/O<sub>3</sub> as a reaction gas.

7. (Currently amended) The method according to claim 1, wherein said inter-metal dielectric layer comprises a BPSG layer, deposited by atmospheric pressure CVD method, utilizing one of TEOS/O<sub>3</sub>, TMPO and TEB as a reaction gas, at a temperature lower than 550°C.

8. (Currently amended) The method according to claim 1, wherein said inter-metal dielectric layer comprises a BPSG layer, deposited by plasma enhanced CVD method, utilizing one of TEOS, O<sub>3</sub>/O<sub>2</sub>, TMP and TMB as a reaction gas, at a temperature between about 400°C and 500°C.